IN THE CLAIMS

Please amend the claims as follows:

1. (original) An active matrix device comprising an array of display pixels (1), each pixel comprising:

a current driven light emitting display element (2);

a drive transistor (T_D) for driving a current through the display element;

first and second capacitors (C_1, C_2) connected in series between the gate (G) and source (S) or drain (D) of the drive transistor (T_D), a data input to the pixel being provided to the junction (30) between the first and second capacitors thereby to charge the second capacitor (C_2) to a voltage derived from the pixel data voltage, and a voltage derived from the drive transistor threshold voltage being stored on the first capacitor (C_1); and

a discharge transistor (A_4) connected between the junction (30) between the first and second capacitors and a common line (26) for all pixels of the display.

2. (original) A device as claimed in claim 1, wherein the drive transistor (T_D) comprises a p-type thin film transistor.

3. (currently amended) A device as claimed in claim 1~~ or 2~~, wherein the drive transistor (T_D) comprises a polysilicon or microcrystalline silicon transistor.

4. (original) A device as claimed in claim 3, wherein the drive transistor (T_D) comprises a low temperature polysilicon transistor.

5. (currently amended) A device as claimed in ~~any preceding claim~~claim 1, wherein each pixel further comprises an input transistor (A_1) connected between an input data line (6) and the junction (30) between the first and second capacitors.

6. (currently amended) A device as claimed in ~~any preceding claim~~claim 1, wherein each pixel is operable in two modes, a first mode in which the input transistor (A_1) is off and the voltage derived from the drive transistor threshold voltage is stored on the first capacitor (C_1), and a second mode in which the input transistor (A_1) is on and a data input to the pixel charges the second capacitor (C_2) to the voltage derived from the pixel data voltage.

7. (currently amended) A device as claimed in ~~any preceding claim~~claim 1, wherein the drive transistor (T_D) is a p-type transistor and the source of the drive transistor is connected to a power supply line (26).

8. (original) A device as claimed in claim 7, wherein the common line comprises the power supply line (26).

9. (currently amended) A device as claimed in ~~any preceding claim~~claim 1, wherein each pixel further comprises a second transistor (A_2) connected between the gate (G) and drain (D) of the drive transistor (T_D).

10. (original) A device as claimed in claim 9, wherein the second transistor (A_2) is controlled by a first gate control line which is shared between a row of pixels.

11. (currently amended) A device as claimed in ~~any preceding claim~~claim 1, wherein the first and second capacitors (C_1,C_2) are connected in series between the gate (G) and source (S) of the drive transistor (T_D).

12. (currently amended) A device as claimed in ~~any preceding claim~~claim 1, wherein each pixel further comprises a third transistor (A_3) connected between the drive transistor and the display element (2).

13. (currently amended) A device as claimed in ~~any preceding claim~~claim 1, wherein the display element (2) comprises an electroluminescent display element.

14. (original) A device as claimed in claim 13, wherein the electroluminescent (EL) display element (2) comprises an electrophosphorescent organic electroluminescent display element.

15. (original) A method of driving an active matrix display device comprising an array of current driven light emitting display pixels (1), each pixel comprising an display element (2) and a drive transistor (T_D) for driving a current through the display element, the method comprising, for each pixel:

isolating a data line (6) from the pixel, and while the data line is isolated:

driving a current through the drive transistor, and charging a first capacitor (C_1) to a resulting gate-source voltage;

discharging the first capacitor (C_1) through a discharge transistor (A_4) connected between one terminal of the first capacitor and a common line, until the drive transistor turns off, the first capacitor (C_1) thereby storing a threshold voltage;

coupling a data line (6) to the pixel, and while the data line is coupled:

charging a second capacitor (C_2), in series with the first capacitor between the gate and source or drain of the drive transistor (T_D), to a data input voltage from the data line (6); and

using the drive transistor (T_D) to drive a current through the display element using a gate voltage that is derived from the voltages across the first and second capacitors (C_1,C_2).

16. (original) A method as claimed in claim 15, wherein the isolating and coupling comprises switching an address transistor (A_1) connected between the data line (6) and an input (30) to the pixel.

17. (original) A method as claimed in claim 16, wherein the address transistor (A_1) for each pixel in a row is switched on simultaneously by a common row address control line.

18. (original) A method as claimed in claim 17, wherein the address transistors for one row of pixels are turned on substantially immediately after the address transistors for an adjacent row are turned off.

19. (currently amended) A method as claimed in ~~any one of claims 15 to 18~~claim 15, wherein when the data line (6) is isolated from the pixel and the first capacitor is being charged, the data line is used to provide a data input voltage to another pixel associated with the data line.

20. (currently amended) A method as claimed in ~~any one of claims 15 to 19~~claim 15, for driving a display device in which each pixel comprises a p-type drive transistor.

21. (currently amended) A method as claimed in ~~any one of claims 15 to 20~~claim 15, for driving a display device in which the drive transistor comprises a polysilicon or microcrystalline silicon transistor.

22. (original) A method as claimed in claim 21, for driving a display device in which the drive transistor of each pixel comprises a LTPS transistor.